EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S12	26610	lookup adj table	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:05
S13	319	(decompos$3) adj function	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:47
S14	3	S12 and S13	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:06
S15	1	S12 and S13 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:06
S16	3279	(decompos$3 divid$4) adj function	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/05/27 18:58
S17	134	S16 and S12	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:08
S18	2	S16 and S12 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:08
S24	38	(decompos$3) adj function and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:54
S25	28	(decompos$3) adj function and (FPGA PLD)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:56
S26	28	(decompos$3) adj function and (FPGA PLD)and mapping and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 15:03
S27	18	(decompos$3) adj function and (FPGA PLD)and mapping and (LUT look-up adj table) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 13:57

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S28	28	(decompos$3) adj function and (FPGA PLD) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 15:52
S29	5	(decompos$3) adj function and (LUT lookup adj table) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 15:55
S30	20	(decompos$3) same function and (LUT lookup adj table) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:11
S31	254	(PLD FPGA programable) and (LUT lookup adj table) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:32
S32	10	(PLD FPGA programable) and (LUT lookup adj table) and (rotat$3 swap$4) adj (input pin)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:13
S33	2271	decompos$3 near4 function	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:32
S34	51055	input near3 variable	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:33
S35	106	S33 and S34	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:34
S36	73602	(LUT or lookup adj2 table or look-up adj2 table)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:35
S37	30	S35 and S36	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:36
S38	20	S37 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:42
S39	164	S33 and S36	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:43

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S40	29	S33 and S36 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 16:45
S42	30	S33 and S36 and S34	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/06 19:14
S45	834	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$4) near4 (input pin terminal)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 07:36
S47	14	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$4) near4 (input pin terminal) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 07:37
S48	2	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$4) near4 (input pin terminal)and (decompos$3 adj2 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:11
S51	186	(decompos$3 split$3 divid$5) near4 function same (LUT or look$3 adj2 table)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 13:28
S52	6	(decompos$3 split$3 divid$5) near4 function same (LUT or look$3 adj2 table)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 13:35
S53	3	(decompos$3 split$3 divid$5) near4 function same (LUT or look$3 adj2 table)and map$4 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 13:36
S54	2	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$4) near4 (input pin terminal)and (decompos$3 near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:13
S55	2	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5) near4 (input pin terminal)and (decompos$3 near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:13
S56	2	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable) near4 (input pin terminal)and (decompos$3 near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:14

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S58	4	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable) near4 (input pin terminal)and ((divid$4 or decompos$3) near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:18
S59	4	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:19
S60	2	(LUT or (lookup adj table) or (look-up adj table))same map$4 and (rotat$3 swap$5 permutable) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:19
S61	15	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 function) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:36
S62	23	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (circuit function)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:41
S63	16	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit function)) and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:43
S64	17	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit region sub-region subregion area subarea function)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:45

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S65	17	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit region sub-region subregion area sub-area function)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:45
S66	18	(LUT or (lookup adj table) or (look-up adj table))and map$4 and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit region sub-region subregion area sub-area function portion)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 18:46
S67	31	(LUT or (lookup adj table) or (look-up adj table)) and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit region sub-region subregion area sub-area function portion)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 19:29
S68	33	(LUT or (lookup adj table) or (look-up adj table)) and (rotat$3 swap$5 permutable chang$3) near4 (input pin terminal)and ((divi$5 or decompos$3) near4 (sub-circuit subcircuit region sub-region subregion area sub-area function$3 portion)) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 19:30
S69	525	map$4 same decompos$5 same function$3	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 19:54
S70	61	map$4 same decompos$5 same function$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 19:55
S71	61	map$4 same decompos$5 same function$3 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 20:03
S72	57	map$4 same decompos$5 same function$3 and "716"/$.ccls. and @ad<"20031027"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 20:04

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S73	0	map$4 same (LUT lookup look-up) same table same decompos$5 same function$3 and "716"/$.ccls. and @ad<"20031027"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 20:06
S74	10	map$4 same (LUT lookup look-up) same table same (divi$5 split$3 decompos$5) same function$3 and "716"/$.ccls. and @ad<"20031027"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 20:11
S75	17	map$4 same (LUT lookup look-up) same table and (divi$5 split$3 decompos$5) near5 function$3 and "716"/$.ccls. and @ad<"20031027"	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/07 20:11
S81	1346	LUT same map$4	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:11
S82	11	LUT same map$4 same decompos$5	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:25
S83	2	LUT same map$4 same decompos$5 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:24
S84	0	LUT same map$4 same decompos$5 near5 function and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:24
S85	77	LUT same map$4 same (divid$3 decompos$5)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:26
S86	3	LUT same map$4 same (divid$3 decompos$5)and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/08 19:26
S87	6	(PLD FPGA programable) and (LUT lookup adj table) and (rotat$3 swap$4) adj (input pin) and map$4 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/09 16:48
S89	24	"5" adj2 input same LUT same "6" adj2 input	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/14 10:51
S90	32	logic same synthesis same LUT	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/12 15:06

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S95	12	"5" adj2 input same "6" adj2 input same (LUT lookup) same logic adj3 block	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/14 11:08
S97	12	("5" "4") near2 input same "6" near2 input same (LUT lookup) same logic adj3 block	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/14 11:16
S98	39	("5" "4") near2 input same "6" near2 input same (LUT lookup) and (logic adj3 block CLB PLB)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/14 11:27
S99	2	("5" "4") near2 input same "6" near2 input same (LUT lookup) and (logic adj3 block CLB PLB) and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2005/09/14 11:25
S100	7393	(PLD FPGA CPLD PLA programmable adj2 device) and (LUT lookup adj table look-up adj table)	US-PGPUB; USPAT; USOCR; DERWENT	OR	ON	2006/05/08 12:48
S101	2145	(decompos$3 de-compos$3) with function and input	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 12:50
S102	91	S100 and S101	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:19
S103	547380	implement$5 and configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 12:51
S104	80	S102 and S103	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 12:55
S105	208305	(rotat$3 swap$4 interchang$3) with (input variable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 12:54

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S106	8	S104 and S105	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:18
S123	86	S100 and S101 and implement$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:35
S124	2084	determin$3 same (de-compos$3 decompos$3) same function	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:39
S125	499	determin$3 same (de-compos$3 decompos$3) with function	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:39
S126	1	determin$3 same (de-compos$3 decompos$3) with function same LUT	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:41
S127	3	determin$3 same (de-compos$3 decompos$3) same function same LUT	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:42
S128	13	determin$3 same (de-compos$3 decompos$3) same function same (look adj2 up adj2 table LUT)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/08 13:42
S130	0	(decompos$3 adj2 function) same (implement5 map$4 configurat$3) same (LUT look adj2 up adj2 table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 15:28

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S132	4	decompos$3 same function same (implement5 map$4 configurat$3) same (LUT look adj2 up adj2 table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 15:49
S133	391	decompos$3 same function and (implement5 map$4 configurat$3) and (LUT look adj2 up adj2 table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 15:49
S135	30	decompos$3 same function same (implement5 map$4 configurat$3) and (LUT look adj2 up adj2 table) and (input variable pin) with (swap$4 rota$3 switch$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 16:26
S136	87	decompos$3 same function and (implement5 map$4 configurat$3) and (LUT look adj2 up adj2 table) and (input variable pin) with (swap$4 rotat$3 switch$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 18:59
S137	2209	(program$5 adj2 (IC integrated adj circuit device) fpga pld pla) same (LUT look adj2 up adj2 table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:03
S138	6081	decompos$3 with function	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:04
S139	1686479	(input variable pin) same (swap$4 switch$3 interchang$3 rotat$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:06
S140	15280	(implement$3 map$4) same (LUT look adj2 up adj2 table)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:08

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S141	52	S137 and S138	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:08
S142	45	S137 and S138 and S139	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:13
S143	20	S137 and S138 and S139 and S140	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:08
S144	0	(determin$3 check$3 fit$4) same (decompos$3 adj2 function) same (LUT look adj2 up adj2 table) same (implement$5 map$4 configurat$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 19:17
S145	638	716/17.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/17 20:31
S147	545799	(rotat$3 swap$4 interchang$3 rearrang$3) with (input variable pin)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:38
S148	169104	(implement$3 synthesi$4 map$4) and (fpga pld programmable)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:46
S149	157344	decompos$5 and (subfunction function)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:53

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S150	6488	(LUT look adj2 up adj2 table) same configur$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:58
S151	3374	S147 and S149	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:59
S152	2736	S148 and S150	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 19:59
S153	8	S151 and S152	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:06
S154	779	decompos$3 adj2 (subfunction sub-function function)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:07
S155	36	S147 and S154	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:12
S156	0	S147 and S154 and S150	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:08
S158	90	S148 and S154	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:12

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S159	12	S148 and S154 and S150	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:14
S160	1285801	(implement$3 map$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:14
S161	5201	S150 and S160	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:15
S162	16	S161 and S154	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:15
S163	54	(map$4 implement$3) and decompos$3 same function and (input variable pin) and (LUT look adj up adj table) same configur$5 and (rota$3 swap$4 rearrang$3 interchang$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/27 20:27
S164	586	716/16.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/05/29 17:13

Terms used
decomposing function implement LUT lookup table

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1 Combinational logic synthesis for LUT based field programmable gate arrays

Jason Cong, Yuzheng Ding
April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2
Publisher: ACM Press

Full text available: pdf(628.91 KB) Additional Information: full citation, abstract, references, citings, index terms, review

The increasing popularity of the field programmable gate-array (FPGA) technology has generated a great deal of interest in the algorithmic study and tool development for FPGA-specific design automation problems. The most widely used FPGAs are LUT based FPGAs, in which the basic logic element is a K-input one-output lookup-table (LUT) that can implement any Boolean function of up to K variables. This unique feature of the LUT has brought new challenges to lo ...

Keywords: FPGA, area minimization, computer-aided design of VLSI, decomposition, delay minimization, delay modeling, logic optimization, power minimization, programmable logic, routing, simplification, synthesis, system design, technology mapping

2 Functional multiple-output decomposition with application to technology mapping for lookup table-based FPGAs

Bernd Wurth, Ulf Schlichtmann, Klaus Eckl, Kurt J. Antreich
July 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 3
Publisher: ACM Press

Full text available: pdf(277.61 KB) Additional Information: full citation, abstract, references, citings, index terms

Functional decomposition is an important technique for technology mapping to look up table-based FPGA architectures. We present the theory of and a novel approach to functional disjoint decomposition of multiple-output functions, in which common subfunctions are extracted during technology mapping. While a Boolean function usually has a very large number of subfunctions, we show that not all of them are useful for multiple-output decomposition. We use a partition of the set of bo ...

Keywords: Boolean functions, FPGA technology, TOS, assignable functions, computer-aided design of VLSI, decomposition, implicit BDD-based methods, mapping synthesis, multiple-output decomposition, preferable functions, subfunction sharing gain, subfunction sharing potential, variable partitioning for decomposition

3 A tutorial on logic synthesis for lookup-table based FPGAs

Robert J. Francis

November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society Press

Full text available: pdf(812.66 KB) Additional Information: full citation, references, citings, index terms

4 BDD-based logic synthesis for LUT-based FPGAs

Navin Vemuri, Priyank Kalla, Russell Tessier

October 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 4

Publisher: ACM Press

Full text available: pdf(379.86 KB) Additional Information: full citation, abstract, references, index terms

Contemporary FPGA synthesis is a multiphase process that involves technology-independent logic optimization followed by FPGA-specific mapping to a target FPGA technology. Conventional technology-independent transformations target standard cells and are unable to optimize circuits with constraints and goals specific to FPGA architectures. This article describes an *FPGA-specific* logic synthesis approach, which unites multilevel logic transformation, decomposition, and optimization technique ...

Keywords: BDD, FPGA, decomposition, logic synthesis

5 Structural gate decomposition for depth-optimal technology mapping in LUT-based FPGA designs

Jason Cong, Yean-Yow Hwang

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Publisher: ACM Press

Full text available: pdf(290.65 KB) Additional Information: full citation, abstract, references, index terms, review

In this paper we study structural gate decomposition in general, simple gate networks for depth-optimal technology mapping using K-input Lookup-Tables (K-LUTs). We show that (1) structural gate decomposition in any K-bounded network results in an optimal mapping depth smaller than or equal to that of the original network, regardless of the decomposition method used; and (2) the problem of structural gate decomposition for depth-optimal tech ...

Keywords: FPGA, computer-aided design of VSLI, decomposition, delay minimization, logic optimization, programmable logic, simplification, synthesis, system design, technology mapping

6 Collision detection and proximity queries

Sunil Hadap, Dave Eberle, Pascal Volino, Ming C. Lin, Stephane Redon, Christer Ericson

August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**

Publisher: ACM Press

Full text available: pdf(11.22 MB) Additional Information: full citation, abstract

This course will primarily cover widely accepted and proved methodologies in collision detection. In addition more advanced or recent topics such as continuous collision detection, ADFs, and using graphics hardware will be introduced. When appropriate the methods discussed will be tied to familiar applications such as rigid body and cloth simulation, and will be compared. The course is a good overview for those developing

applications in physically based modeling, VR, haptics, and robotics.

7 Series-parallel functions and FPGA logic module design

Shashidhar Thakur, D. F. Wong
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press

Full text available: pdf(282.20 KB) Additional Information: full citation, abstract, references, citings, index terms

The need for a two-way interaction between logic synthesis and FPGA logic module design has been stressed recently. Having a logic module that can implement many functions is a good idea only if one can also give a synthesis strategy that makes efficient use of this functionality. Traditionally, technology mapping algorithms have been developed after the logic architecture has been designed. We follow a dual approach, by focusing on a specific technology mapping algorithm, namely, the struc ...

Keywords: field programmable gate arrays, series-parallel technology mapping, tree-based technology mapping algorithm, universal logic modules

8 An efficient framework of using various decomposition methods to synthesize LUT networks and its evaluation

Shigeru Yamashita, Hiroshi Sawada, Akira Nagoya
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Publisher: ACM Press

Full text available: pdf(110.08 KB) Additional Information: full citation, references

9 Separable image warping with spatial lookup tables

G. Wolberg, T. E. Boult
July 1989 **ACM SIGGRAPH Computer Graphics , Proceedings of the 16th annual conference on Computer graphics and interactive techniques SIGGRAPH '89**, Volume 23 Issue 3
Publisher: ACM Press

Full text available: pdf(1.99 MB) Additional Information: full citation, abstract, references, citings, index terms

Image warping refers to the 2-D resampling of a source image onto a target image. In the general case, this requires costly 2-D filtering operations. Simplifications are possible when the warp can be expressed as a cascade of orthogonal 1-D transformations. In these cases, separable transformations have been introduced to realize large performance gains. The central ideas in this area were formulated in the 2-pass algorithm by Catmull and Smith. Although that method applies over an important cla ...

10 Technology mapping issues for an FPGA with lookup tables and PLA-like blocks

Alireza Kaviani, Stephen Brown
February 2000 **Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays**
Publisher: ACM Press

Full text available: pdf(612.01 KB) Additional Information: full citation, abstract, references, index terms

In this paper we present new technology mapping algorithms for use in a programmable logic device (PLD) that contains both lookup tables (LUTs) and PLA-like blocks. The technology mapping algorithms partially collapse circuits to reduce either area or depth, and pack the circuits into a minimum number of LUTs and PLA-like blocks. Since no other technology mapping algorithm for this problem has been previously published, we cannot compare our approach to others. Instead, to illustrate the im ...